Electronic Version
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Claims

[c1] What is claimed is:

1.A method of forming at least one wire on a substrate, the substrate comprising at least one conductive region, an insulating layer disposed on the substrate, and the insulating layer comprising at least one recess exposing the conductive region, the method comprising:

forming a barrier layer on a surface of the insulating layer and the recess;

forming a continuous and uniform conductive layer on a surface of the barrier layer;

forming a seed layer on a surface of the conductive layer; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up the recess.

[c2] 2.The method of claim 1 wherein the substrate comprises a semiconductor wafer or a silicon-on-insulator substrate (SOI substrate).

[c3] 3. The method of claim 1 wherein the conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor.

[c4] 4.The method of claim 1 wherein the recess is a via hole of a dual damascene structure.

[c5] 5. The method of claim 1 wherein the barrier layer comprises a silicon nitride layer, a titanium nitride layer (TiN layer), a tantalum nitride layer (TaN layer), or a tantalum nitride/tantalum (TaN/Ta) composite metal layer.

[c6] 6.The method of claim 1 wherein the conductive layer comprises an aluminum layer (Al layer) or a tungsten layer (W layer).

[c7] 7.The method of claim 1 wherein a thickness of the conductive layer ranges from 5 to 400 angstroms (Å).

[c8] 8.The method of claim 1 wherein the method for forming the conductive layer comprises a chemical vapor deposition (CVD) process or an atomic layer deposition ALD) process.

[c9] 9.The method of claim 1 wherein the seed layer is a copper layer formed by a physical vapor deposition (PVD) process.

[c10] 10.The method of claim 1 wherein the seed layer is a copper alloy layer formed by a physical vapor deposition (PVD) process.

[c11] 11.The method of claim 1 wherein a thickness of the seed layer ranges from 5 to 2000 angstroms (Å).

[c12] 12.The method of claim 1 wherein the metal layer is formed by an electric copper plating (ECP) process.

[c13] 13.A method of forming at least one dual damascene wire on a substrate, the substrate comprising at least one conductive region, an insulating layer disposed on the substrate, and the insulating layer comprising at least one trench pattern and via hole pattern stacked from top to bottom exposing the conductive region, the method comprising:
forming a barrier layer on a surface of the insulating layer, the trench pattern, and the via hole pattern;
forming a continuous and uniform conductive layer on a surface of the barrier layer;
forming a seed layer on a surface of the conductive layer; and
forming a metal layer on a surface of the seed layer, and the metal layer filling up the trench pattern and the via hole pattern.

[c14] 14.The method of claim 13 wherein the substrate comprise a semiconductor wafer or a silicon-on-insulator substrate (SOI substrate).

[c15] 15.The method of claim 13 wherein the conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor.

[c16] 16.The method of claim 13 wherein the barrier layer comprises a silicon nitride layer, a titanium nitride layer (TiN layer), a tantalum nitride layer (TaN layer), or a tantalum nitride/tantalum (TaN/Ta) composite metal layer.

[c17] 17.The method of claim 13 wherein the conductive layer comprises an aluminum layer (Al layer) or a tungsten layer (W layer).

[c18] 18.The method of claim 13 wherein the method for forming the conductive layer comprises a chemical vapor deposition (CVD) process or an atomic layer deposition (ALD) process, and a thickness of the conductive layer ranges from 5 to 400 angstroms (Å).

[c19] 19.The method of claim 13 wherein the seed layer is a copper layer formed by a physical vapor deposition (PVD) process, and a thickness of the seed layer ranges from 5 to 2000 angstroms (Å).

[c20] 20.The method of claim 13 wherein the seed layer is a copper alloy layer formed by a physical vapor deposition (PVD) process, and a thickness of the seed layer ranges

from 5 to 2000 angstroms (Å).

[c21] 21.The method of claim 13 wherein the metal layer is formed by an electric copper plating (ECP) process.